ABSTRACT OF THE DISCLOSURE

In a nonvolatile memory, the select gates (144S) are formed from one conductive layer (e.g. polysilicon or polyside), and the wordlines (144) interconnecting the select gates are made from a different conductive layer (e.g. metal). The wordlines overlie an interlevel dielectric (310) formed over control gates (134). The dielectric thickness can be controlled to reduce the capacitance between the wordlines and the control gates. In some embodiments, the floating gates (120) are fabricated in a self-aligned manner using an isotropic etch of the floating gate layer.